IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of **Ham III**	)	Patent Pending
Serial No.: 09/747,052	)	Examiner: Ted M. Wang
Filed: 22 December 2000	)	Group Art Unit: 2611
For: **CLOCK SYNCHRONIZATION IN A COMMUNIATIONS ENVIRONMENT**	)	Confirmation No.: 1573

Docket No: 4015-808

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26 October 2006 — Date

Laura A. Wade — Laura A. Wade

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APPEAL BRIEF

Dear Sir or Madam:

This appeal brief is timely filed within one month of the Office's 26 September 2006 mailing of the Notice of Panel Decision from Pre-Appeal Brief review. Thus, no extension-of-time fees should be required for its entry. Applicant submits herewith payment in the amount of $500 to cover the appeal brief fee. If any further fees or charges are required, the Commissioner is hereby authorized to charge them to Deposit Account 18-1167.

I. REAL PARTY IN INTEREST

The real party in interest is Ericsson Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences to the best of Applicant's knowledge.

III. STATUS OF CLAIMS

Claims 1-7, 10-16, 18, 24-26, 32-35, 37, and 39 stand rejected by the examiner. Claims 8, 9, 17, 19-23, 27-31, 36, and 38 are objected to as allowable but for their dependence on a rejected base claim. Accordingly, Applicant appeals the rejection of claims 1-7, 10-16, 18, 24-26, 32-35, 37, and 39.

IV. STATUS OF AMENDMENTS

All amendments have been entered to the best of Applicants' knowledge.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The pending claims under appeal include claims 1-7, 10-16, 18, 24-26, 32-35, 37, and 39, which include independent claims 1, 10, and 24. Applicant asserts that no dependent claims under appeal are in means-plus-function form under 35 U.S.C. §112, ¶ 6, and thus summarizes only the independent claims under appeal in accordance with 37 C.F.R. § 41.37(v) and (vii).

A. Independent claim 1

Independent method claim 1 is directed to generating an output clock signal from a phase-locked-loop (PLL) where the phase differences between an input reference clock signal and the output clock signal are filtered to produce frequency control values for the PLL, and where that filtering is adapted based on an average of the frequency control values. The Office Action response submitted by Applicant on 27 Feb. 2006

included amendments to claim 1, clarifying that the claimed output clock signal was the final output signal from the PLL as opposed to any signal internal to the PLL circuit.

That claimed distinction of a "final" output clock signal is important, as illustrated in Fig. 5, depicting a PLL module 62 that generates a clock output signal from a clock input signal in accordance with the limitations of claim 1. As shown in Fig. 4, the PLL module 62 may comprise part of a radio head interface (RHI) 50, which provides the output clock signal as a carrier frequency reference signal to a downstream radio transmitter 52 (shown in Fig. 3).

Exemplary operation of a PLL circuit operating according to the limitations of claim 1 appears in the specification at p. 9, lines 9 – 24. That section explains that the PLL module 62 generates a phase error signal by determining a phase difference between the reference clock signal and a feedback signal, which is driven by the output clock signal. The specification additionally explains that a loop filter 68 operates on the phase error signal to generate a control value and that, in turn, the control value determines the value or magnitude of an oscillator control signal generated by an oscillator controller 72. An oscillator 74 generates the output clock signal at a frequency determined by the oscillator control signal.

Of particular relevance to the limitations of claim 1, the specification at p. 10, lines 18-24, explains that control logic 70 operates on the control values being output by the loop filter 68 to determine when and how to update the loop filter 68. Specifically, the control logic 70 adapts the loop filter 68, which changes the frequency response and sensitivity of the PLL module 62, based on filtered (averaged) control values output by the loop filter 68. Thus claim 1 describes a PLL circuit that generates an output clock signal for downstream circuitry based on control values representing a filtered phase error signal, but where, importantly, the filter response of the loop filter 68 is controlled based on an average of those same control values.

The processing logic of Fig. 7 provides a further example of overall PLL modulation operation and loop filter adaptation based on averaging the control values output by the loop filter. See, e.g., the specification at lines 15-23, explain Steps 200-212 of PLL module operations. In particular, Step 208 stipulates that control logic 70 sets/maintains the operating state of the PLL module 62—i.e., sets/maintains the loop filter characteristics of the loop filter 68—based on processing the control values output by the loop filter 68.

B. Independent claim 10

Independent method claim 10 corresponds closely with independent method claim 1 in that it explicitly claims a method of generating an output timing signal—e.g., an output clock signal—in a PLL that is referenced to an input timing signal—e.g., a reference clock signal. However, claim 10 further includes an explicit limitation to determining average control values by averaging successive digital control values, such as those generated by the loop filter 68 shown in Figure 5 and described at p. 9, lines 14-17. Moreover, claim 10 explicitly claims adapting a filter characteristic of the digital filter used to generate the digital control values, based on the average control values.

An exemplary description for a digital implementation of the loop filter 68 appears in the specification at p. 11, line 10 – p. 12, line 2. That section explains that the loop filter 68 may be configured as a proportional-integral filter, which outputs digital count values as the claimed control values.

As one example of the adaptation of loop filter 68 as claimed in claim 10, the specification at p. 12, lines 3 – 10, explains that eliminating clock deviations in the output clock signal may be accomplished by basing loop filter adaptations on the average digital control values. Figure 6 and the specification at p. 13, lines 10-16, identify example operating states for the PLL module 62, and illustrate the desirability of

changing the filter response of the loop filter 68 as a function of operating conditions, which may be gleaned by observing averages of the control values

See, especially, the discussion at p. 14, lines 6 – 15, wherein the specification explains the various deductions that may be made regarding stability or "lock" conditions of the PLL module 62, based on observing the behavior of the average of the control values output by the loop filter 68. See, also, p. 16, lines 5 – 14, for additional discussion explaining loop filter adaptation based on averaging the control values output by the loop filter 68. See, also, the processing logic of Fig. 7 and p. 16, lines 15 – 23 of the specification explained in the last paragraph of the preceding summary given for claim 1.

C. Independent claim 24

Independent apparatus claim 24 claims a PLL having features like or similar to those claimed in independent method claims 1 or 10. As with claim 1, Applicant submitted amendments in the office action response of 27 Feb. 2006, to better clarify that the claimed output (clock) signal from the PLL was an output from the PLL, rather than any internal feedback or control signal within the PLL.

Referring to Fig. 5 and p. 9 of the specification, claim 24 claims a PLL 62 comprising a controllable oscillator 74 that provides an output signal from the PLL 62 at a frequency proportionate to an oscillator control signal (generated by an oscillator controller 72). Claim 24 further claims a phase detector 66 that provides a phase error signal by detecting a phase difference between an input (clock) signal and an output (clock) signal. Claim 24 further claims an adjustable loop filter 68 that provides control values based on filtering the phase error signal (from the phase detector 66), and a control circuit (controller) 72 that provides the oscillator control signal responsive to the control values.

Of more particular interest to the patentability arguments appearing later herein, claim 24 further claims control logic 70 to control a filter characteristic of the loop filter 68

based on an average control value determined from successive ones of the control values output by the loop filter 68. Doing so minimizes clock deviations in the output clock signal.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The examiner rejects 1-7, 10, 11, 13-16, 18, 24-26, 32, and 37 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,909,148 to Tanaka (hereinafter "Tanaka").

The examiner rejects claims 34, 35, and 39 under 35 U.S.C § 103(a) as being anticipated by Tanaka in view of U.S. Patent No. 6,353,647 to Wilhelmsson et al. (hereinafter "Wilhelmsson").

The examiner rejects claims 12 and 33 under 35 U.S.C § 103(a) as being anticipated by Tanaka in view of U.S. Patent No. 5,619,543 to Glass et al. (hereinafter "Glass").

VII. ARGUMENT

A. All anticipation rejections rely on improper claim construction

The anticipation rejections of independent claims 1, 10, and 24 rely on a legally erroneous claim construction by the examiner. Fundamentally, the examiner's anticipation arguments may be understood as asserting that the signal output by the Numerical Controlled Oscillator (NCO) 9 shown in Figure 1 of Tanaka is the PLL output signal claimed in claims 1, 10, and 24, and is generated in a like manner for a like purpose. See, e.g., p. 4 of the Final Office Action for the examiner's rebuttal to Applicant's argument that Applicant's claimed PLL output signals cannot be construed as encompassing internal circuit feedback signals generated by NCO 9 in Tanaka.

Further, note that the examiner argues that Applicant's claimed PLL output signal and the NCO 9 signal of Tanaka are the same for claim interpretation purposes based on "Figure C" at p. 6 of the Final Office Action. Figure C represents an arbitrary rearrangement of Figure 1 in Tanaka, where the examiner incorrectly re-labels the NCO 9 signal as an output frequency signal. Tanaka's detailed teachings regarding the NCO 9 signal do not support the examiner's drawing and arguments. See, e.g., Tanaka at col. 4, lines 60 – 65, which state that the *input* signal to NCO is proportional to the output frequency (of Tanaka's overall carrier phase synchronization circuit). Figure 1 of Tanaka labels the overall output signal as the "DEMODULATED SIGNAL." Thus, it is error to label NCO 9's *output* signal as the "output frequency signal."

Note also, that Figure C of the Final Office Action shows the "output frequency signal" of NCO 9 as being the g(nT) signal taught by Tanaka. That labeling is plain error, as Tanaka illustrates g(nT) being the *input* signal to NCO 9, not its *output*. See, also, Tanaka at col. 4, lines 66 – 67, plainly stating that g(nT) is generated by Tanaka's loop filter 11, and not output by NCO 9 as the examiner's Figure C alleges. Moreover, Tanaka explains at col. 5, lines 43-50 that the "oscillating frequency of NCO 9 is controlled so that it [its output signal] becomes the residual frequency error of the AFC loop."

Thus, the Final Office Action uses a drawing that plainly contradicts the actual teachings of Tanaka to argue that the NCO 9 signal is the same as Applicant's claimed PLL output signal, for purposes of claim construction. Not only is the NCO 9 signal not generated in the same manner as Applicant's claimed PLL output signal, it unambiguously is a feedback loop signal internal to carrier phase synchronization circuit shown in Figure 1 of Tanaka and discussed throughout.

In contrast, the "*output clock signal from the PLL*" of claim 1, the "*output signal generated by the PLL*" of claim 10, and the "*output signal from the PLL*" of claim 24 are output signals from the PLL at issue. For example, Figure 3 of the specification

illustrates a radio head interface (RHI) 50 providing a timing output signal for a downstream radio transceiver (TRX) 52, and Figure 4 illustrates that a PLL module 62 in the RHI 50 generates that output clock signal for the TRX 52. (See the specification at p. 8, lines 14 – 15; and at p. 8, line 24 – p. 9, line 8.)

With these plain teachings in the specification reinforcing the ordinary meaning of the output signal claimed in claims 1, 10, and 24, one of ordinary skill in the art would not interpret the claim output signal as encompassing the internal feedback signal from NCO 9 in Tanaka. Therefore, it is erroneous for the examiner to construe the claimed output signal as encompassing the internal feedback signal from NCO 9 in Tanaka because that construction is at direct odds with the requirement to construe a claim term "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364, 70 USPQ2d 1827, 1834 (Fed. Cir. 2004). That is, the "broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).

Thus, while Applicant appreciates that the Patent Office must give pending claims their "broadest reasonable interpretation," it notes that interpretation must be "consistent with the specification." Manual of Patent Examining Procedure (MPEP) § 2111 (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005)). The examiner's interpretation of the PLL output signal claimed in claims 1, 10, and 24 is legally wrong because it is inconsistent with the specification and inconsistent with the meaning that one of ordinary skill in the art would give in light of the specification. For this reason alone, all anticipation rejections based on Tanaka fail as a matter of law and should be withdrawn.

B. Tanaka does not anticipate independent claim 1 or any of its dependents.

In generating the claimed PLL output signal, claim 1 includes the limitations of determining successive phase difference values between a reference clock signal and the (PLL) output clock signal, filtering the successive phase difference values to generate successive control values, controlling a frequency of the output clock signal based on the successive control values, and adapting a filter used to filter the successive phase difference values based on average control values determined from the successive control values. For Tanaka to anticipate claim 1, it must set forth each and every one of the foregoing claim limitations. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The examiner argues that Tanaka teaches the determining limitation of claim 1 at p. 9 of the Final Office Action. There, the examiner states that elements 8 and 10 of Tanaka teach claim 1's limitation of determining successive phase differences between a reference clock signal and an output clock signal because "*it is inherent that the NCO output* [of NCO 9 in Tanaka] *can be taken as an output clock signal.*" As earlier argued, it is legal error to state that the NCO 9 output can be taken as the PLL output signal within the meaning of the claim.

In some arbitrary sense, disconnected from the claim context—indeed, disconnected from Tanaka's context—the NCO 9 signal can be viewed as an output clock signal with respect to NCO 9, but it cannot be viewed as an output clock signal with respect to Tanaka's carrier phase synchronization circuit or to Applicant's claimed PLL. This use of the internally generated feedback signal of NCO 9 in advancing the anticipation argument make clear that Tanaka does not disclose an invention identical to or in as complete detail as is presented in claim 1, which is required by law. See MPEP

§ 2131.02 (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Nor does Tanaka teach the filter adapting limitation of claim 1. As taught by the specification at p. 9, lines 5 – 24, for example, the claimed filter adaptation is an adaptation of the loop filter 68, which generates control values based on filtering phase error differences detected by the phase detector 66. Control logic 70 filters (averages) these control values to determine how and when to update the loop filter 68. Thus, the control values that are used ultimately to set the PLL output frequency themselves are filtered phase error signal values, and an averaged version of the control values is used to control phase error signal filtering.

On p. 9 of the Final Office Action, the examiner asserts that elements 13, 14, 15, 16, 101, and 102 of Tanaka teach the claimed filter adaptation limitation of claim 1. As Tanaka explains at col. 4, lines 3 – 23, elements 13, 14, 15, and 16 cooperate to provide a change amount value of the AFC residual frequency error for a predetermined time period. In other words, these elements in Tanaka determine whether the residual frequency error changes by more than a certain amount over a certain time period. The resulting control signal is used to access a memory 101, which includes loop parameters for setting the loop filter 11 via PLL controller 102.

Thus, Tanaka teaches detecting the change amount of residual AFC frequency error relative to a predetermined time, as a control basis for PLL loop adaptation. Such control cannot be said to anticipate the claimed limitation of adapting a (PLL) loop filter based on averaging the PLL frequency control values output by that loop filter, as is explicitly claimed in claim 1.

At least for the reasons given above, Tanaka fails as a matter of law to anticipate claim 1. As such, the rejection of claim 1 (and any of its dependents) should be withdrawn.

C. Tanaka does not anticipate claims 2-4.

Claim 2 claims detecting a trend in the average control values determined from the control values output by the loop filter in claim 1, and includes the limitation of setting a PLL loop filter state based on the determined trend. (See, for example, the specification at p. 22, lines 22+ for a discussion of trend-based control; see, also, Figure 13 and the the specification at p. 23, lines 16+.)

The anticipation rejection states that Tanaka teaches detecting a trend in the manner claimed at col. 3, line 58 – col. 4, line 18, and at col. 5, line 40 – col. 6, line 25. That assertion is unsupported by Tanaka.

The cited sections of Tanaka do not teach averaging the control values output by a PLL loop filter and detecting a trend in that average for loop filter adaptation. Rather, as the cited sections explain, Tanaka teaches a filter element 11 that is updated from a memory element 101 based on elements 13, 14 determining the amount that the output of filter element 11 changes over a predetermined time D (as set by element 13). More particularly, element 15 averages the change amounts, and element 16 uses the average of the change amounts—explicitly not the average of the actual output values from filter element 11—to control which update parameters are retrieved from memory element 101 by the PLL controller 102 to update the filter element 11.

Because Tanaka does not teach the limitations of claim 1, much less the trending limitations of claim 2, Tanaka fails to anticipate claim 2 as a matter of law. Likewise, Tanaka fails to anticipate claims 3 and 4, which add further trending-based limitations.

D. Tanaka does not anticipate claims 5-7.

Claim 5 claims determining difference values between successive ones of the average control values, which are themselves determined from the control values output by the PLL loop filter of claim 1, and then controlling PLL loop filter adaptation based on

the average control value differences. See, for example, the specification at p. 17, lines 2 – 5, and Figure 11.

Notably, Tanaka does not compute average control values from the actual control values output by a PLL loop filter, and thus cannot be said to compute differences in the average control values as claimed. That is, the claimed difference values represent successive average control value differences, and not the change amounts produced by elements 13 and 14 of Tanaka. (As Tanaka explains, the change amounts reflect how much the output of filter element 11 has changed over a predetermined time "D" as set by element 13, which relates to the AFC locking time of Tanaka's carrier phase synchronization circuit.)

Regarding the rejection of claim 5, the examiner repeats the basic anticipation rejection argument; namely, that elements 13, 14, 15, 16, 101, and 102 of Tanaka, along with the corresponding specification descriptions in Tanaka teach the claimed limitations. That assertion is erroneous but interesting for the simple reason that when rejecting independent claims 1, 10, and 24, the examiner asserts that these very same elements compute the average of the control values output by Tanaka's filter element 11 and control the filter characteristics of element 11 on that basis. In rejecting claim 5, the examiner asserts that these elements first compute average control values as claimed in claim 1, and then compute differences in those average control values as claimed claim 5, and then control the filter characteristics of filter element 11 based on those differences.

It is self-evident from Tanaka's Figure 1 and from the corresponding descriptions in Tanaka's specification, that subtraction element 14 and delay element 13 cooperate to produce "change amounts," which reflect the amount by which the output of filter element 11 has changed over the predetermined time period D. Those change values are filtered by element 15. The change values are not control values as output by filter

element 11, and the averaged change values of Tanaka are not averaged control values within the meaning of applicant's claims. Tanaka therefore does not teach the limitations of claim 5 and therefore cannot anticipate claim 5.

Regarding claim 6, the examiner admits that Tanaka does not provide its teachings, but argues that it would be obvious to perform the claimed integration. The examiner cannot state that Tanaka anticipates claim 6, while admitting that Tanaka does not teach the limitations of claim 6. The use of "Official Notice" here by the examiner is not well taken.

As Section 2144.03 of the MPEP cautions, "Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances." Specifically, the MPEP cautions examiners that official notice without documentary support may be relied on only in those rare circumstances "where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." More emphatically, "the notice of facts beyond the record which may be taken by the examiner must be 'capable of such instant and unquestionable demonstration as to defy dispute'." *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970) (citing *In re Knapp Monarch Co.*, 296 F.2d 230, 132 USPQ 6 (CCPA 1961)).

Here, the rejection of claim 6 as anticipated by the examiner is tantamount to taking official notice that the detailed teachings regarding the AFC/PLL control loop including elements 11, 13, 14, 15, 16, 101, and 102 of Tanaka are "obviously" modified by one of skill in the art to include the averaged control value integration limitations of claim 6. That assertion flies in the face of the basis for taking official notice without documentary support. Tanaka carefully describes a precision carrier phase synchronization circuit, whose feedback control is based on averaging the amount by which the output from filter element 11 changes over a predetermined time period D. It is

rank speculation for the examiner to suggest that the integration limitations of claim 6 somehow obviously fit into Tanaka.

Regarding claim 7, claim 7 includes limitations directed to setting the PLL filter to a slow filter state if the integrated value generated in claim 6 is below a predefined threshold. Tanaka does not teach averaging PLL loop filter control values as claimed in claim 1, does not teach determining differences in those averages as claimed in claim 5, does not teach integrating the determined differences as claimed in claim 6, and unequivocally does not teach setting the PLL loop filter to a slow state if the integrated value is below a predefined threshold as claimed in claim 7.

In supporting the anticipation rejection, the examiner states that the limitations of claim 7 are found in Tanaka at col. 4, lines 1 -23, col. 5, line 56 – col. 6, line 23, and element 16 of Figure 1. These sections do no more than identify the basic feedback control loop workings of Tanaka as explained herein. Not a single word or illustration in Tanaka provides any teachings that identify, mention, or relate to controlling a PLL filter as claimed in claim 7.

E. Tanaka does not anticipate independent claim 10 or any of its dependents

Claim 10 is directed to a method of controlling a phase-locked loop (PLL) to reduce clock deviations in an output signal generated by the PLL relative to clock deviations in an input reference timing signal to the PLL. Its limitations include generating a phase error signal by determining a phase difference between the input reference timing signal and the output signal, filtering the phase error signal with a digital filter to produce a digital control value, determining average control values by averaging successive ones of the digital control value, and adapting a filter characteristic of the digital filter based on the average control values.

Tanaka does not teach averaging digital control values output by a PLL loop filter, and therefore cannot anticipate claim 10. Regarding claim 10, the examiner's anticipation rejection simply states that all limitations of claim 1 are contained therein, and that the claim 1 rejection arguments thus apply. (See p. 11 of the Final Office Action.)

As such, the examiner's rejection of claim 10 must be understood as resting on the assertion that the signal from NCO 9 of Tanaka is the claimed PLL output signal, and that elements 13, 14, 15, 16, 101, and 102 teach the claimed limitations of determining average control values and adapting the loop filter characteristics based on those control values.

The output signal of claim 10 explicitly is an output from the PLL of claim 10. It is legal error for the examiner to equate the claimed output signal with the internal feedback signal from NCO 9 of Tanaka, as doing so violates the requirement that terms in pending claims be construed in a manner consistent with the specification. *Phillips,* 415 F.3d at 1316. More particularly, the examiner commits legal error by failing to give the claim term "output signal" a construction that is consistent with the interpretation that those skilled in the art would reach. *Cortright,* 165 F.3d at 1359.

Tanaka further fails to anticipate claim 10 because elements 13, 14, 15, 16, 101, and 102 in Tanaka do not carry out the alleged limitations of determining average control values (from the control values output by the claimed PLL loop filter), and adapting that PLL loop filter based on the average control values. As earlier detailed, col. 4, lines 8+ of Tanaka state that elements 13 and 14 provide "change amounts" of the smoothed phase error information output by filter 11 of Tanaka—i.e., Tanaka explicitly subtracts the phase error information output by element 11 at an earlier time from the currently output phase error information output by element 11, where the time delay is given by "D" of element 13. Element 15 is noted as averaging these values, but the values being

averaged are not the outputs of filter 11, but rather the time-qualified change amounts from the filter 11. Element 16 uses the average of the time qualified change amounts to access a memory 101, which outputs corresponding loop update parameters to filter 11.

Again, these operations are superficially similar to those claimed in claim 10, but filter 11 and NCO 9 are part of the internal feedback signal generation of the phase synchronization circuit of Tanaka, and thus are not generating the claimed PLL output signal and, just as significantly, do not carry out the claimed control value averaging and loop filtering adapting. By failing to teach or suggest these limitations, Tanaka fails to anticipate claim 10 as a matter of law.

F. Tanaka does not anticipate claims 13-16 and 18.

Claims 13-16 and 18 depend from claim 10 and include limitations directed to determining difference values between average control values, which themselves are determined from the actual control values output by the claimed PLL loop filter, and integrating those differences as a basis for adapting the PLL loop filter. See, e.g., Figure 11 and p. 21, line 14 – p. 23, line 15, for details regarding the specific limitations of claims 13-16 and 18.

Tanaka does not teach averaging the control values output by a PLL loop filter as is required in claim 10, and does not teach determining differences in those average control values as is required in claim 13. Moreover, nowhere does Tanaka mention integrating differences in average control values, as is further required in claim 13.

Notably, the examiner's rejection argument simply states that the rejection arguments made against claim 6 apply. Thus, as best Applicant can understand, the examiner rejects claim 13 on Official Notice that it would be obvious to include the claimed integration limitations of 13 in Tanaka, as integration and averaging are equivalent with respect to filtering element 15 in Tanaka.

In addition to its misuse of Official Notice, this rejection argument overlooks the fact that Applicant claims the additional step of integrating difference values obtained from averaging control values. Thus, however one might speculate about configuring filter element 15 of Tanaka as an integrator, Tanaka does not teach taking an average of loop filter control values, differencing those averages, and *then* integrating the differences. Absent those teachings, it is plain legal error for the examiner to assert that Tanaka anticipates claim 13, or any of claims 14-16 and 18 depending from it.

G. Tanaka does not anticipate independent claim 24 or any of its dependents.

Claim 24 is directed to a phase-locked loop (PLL). The claimed PLL includes a controllable oscillator providing an output signal from the PLL at a frequency proportionate to an oscillator control signal, a phase detector providing a phase error signal by detecting a phase difference between an input signal and the output signal, and an adjustable loop filter providing control values based on filtering the phase error signal. The PLL further includes a control circuit providing the oscillator control signal responsive to the control values, and control logic to control a filter characteristic of the loop filter based on an average control value determined from successive ones of the control values to minimize clock deviations in the output signal.

Tanaka does not teach a PLL that includes control logic that controls filter characteristics of the PLL loop filter based on an average control value determined from successive ones of the control values generated by the PLL loop filter. Regarding claim 24, the examiner's anticipation rejection at p. 13 of the Final Office Action states that Tanaka's elements 101 and 102, col. 4 lines 1-18, and col. 6, lines 1-25 disclose the claimed control logic to control the PLL loop filter characteristics based on an average control value determined from successive ones of the control values output by the claimed PLL loop filter.

That assertion is in error. Element 101 of Tanaka is a memory that does include filter paramters for (filter) element 11 of Tanaka, but the retrieval of those parameters by PLL controller 102 is based on elements 13 and 14 cooperating to obtain "change amounts" of the output from element 11—i.e., values obtained by subtracting the current output value of element 11 from an earlier output value of element 11. (The value of "D" in element 13 sets the predetermined amount of time delta used for the subtraction.) These change amount outputs reflect the change in AFC residual frequency error over the predetermined time period—see Tanaka at col. 6, lines 49-67 for a plain explanation of these operations.

Thus, element 15 averages the change amount outputs from element 14 and explicitly does not average successive output values from element 11. Put simply, the examiner's anticipation rejection rests on the assertion that "successive control values" output by filter element 11 are averaged by element 15 and used by element 101/102 to update filter element 11. Tanaka's teachings do not support, and in fact contradict, that assertion.

Because Tanaka fails to teach the control value averaging and corresponding filter adapting limitations of the claimed control logic, Tanaka fails to anticipate claim 24 as a matter of law.

H. Tanaka does not render claims 34, 35, and 39 obvious.

Applicant notes that the examiner does not allege that Wilhelmsson provides any teachings relevant to the PLL loop filter output control value averaging and corresponding PLL loop filter adaptations present in independent claim 24, nor does Wilhelmsson provide such teachings. Therefore, with those teachings absent from Tanaka, as argued for the independent claims, the combination of Tanaka with Wilhelmsson cannot render obvious any claims depending from claim 24. As such, as a

matter of law, claims 34, 35, and 39, all depending from independent claim 24, are not obvious over the combination of Tanaka and Wilhelmsson.

Moreover, regarding claim 39, the examiner rests the obviousness rejection on the assertion that one would combine Wilhelmsson's teachings with Tanaka's because it would reduce board size and therefore reduce circuit cost. As a statement of motivation to combine, that falls far short of the legal requirements for making out a *prima facie* case of obviousness.

As explained in Section 2142 of the MPEP, the examiner bears the initial burden of making out a prima facie case of obviousness under 35 U.S.C. § 103. As set forth in that section of the MPEP, establishing the prima facie case depends on meeting three basic criteria: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference (or references when combined) must teach or suggest all the claim limitations.

As previously argued, Tanaka plus Wilhelmsson do not teach all the limitations of independent claim 24, and therefore do not render any of claims 34, 35, or 39 obvious. Further, however, with respect to the examiner's obviousness rejection, the determination of whether there is a motivation or suggestion to combine references is a factual question based on specific findings. *In re Gartside*, 203 F.3d 1305, 53 USPQ2d 1769 (Fed. Cir. 2000). On that point, the substantive question is whether one of ordinary skill in the art would have been motivated to combine the references in question. *Winner International Royalty Corp. v. Wang*, 202 F.3d 1340, 53 USPQ2d 1580 (Fed. Cir. 2000).

As motivation for combining Wilhelmsson, the examiner simply states that one would make the combination to reduce circuit size and save cost. That assertion is specious and without support. For example, Tanaka discloses both digital and analog processing—see LPF 1 and A/D Converter 2 of Figure 1 in Tanaka. Tanaka further discloses complex digital signal processing for residual frequency error determination at co. 4, lines 24 – 67. Against this framework, it is unclear which parts of Tanaka the examiner means to "digitize and cost-reduce" by way of Wilhelmsson's teachings.

What, if anything, Wilhelmsson adds to Tanaka is patently unclear on the record. In short, the proffered motivation to combine is self-serving speculation and is not supported in any way by the references, and therefore fails as a matter of law.

I. Tanaka does not render claims 12 33 obvious.

The examiner rejects claim 12 as obvious over the combination of Tanaka and Glass. Claim 12 includes the limitation that the digital filter from claim 10 is a proportional-integral (P-I) digital filter, and further includes the limitation of adapting a filter characteristic of the digital filter based on the average control values based on changing a value of a proportional digital filter coefficient Kp and an integral digital filter coefficient Ki.

Notably, Tanaka offers no teachings on the use of proportional-integral filtering. However, the examiner states that Glass provides proportional-integral filter teachings in accordance with the detailed limitations, and that it would be obvious to modify Tanaka's digital filter circuit (presumably, filter element 11) in view of Glass's teachings.

First, the proffered motivation to combine is legally insufficient, as it represents mere speculation by the examiner that clock jitter in Tanaka would be improved by incorporation of Glass's teachings. One might just as easily speculate that Tanaka already configures its filter element 11 as a proportional-integral filter, although Tanaka does not disclose such details.

However, even if Tanaka is so modified (or inherently operates in the alleged manner), neither Glass nor Tanaka teach adapting proportional-integral filter coefficients as a function of the average of the control values being output by the filter at issue. Without providing these teachings, the combination of Tanaka and Glass as a matter of law cannot render claim 12 obvious.

Claim 33 includes similar limitations for a digital loop filter implemented as a proportional-integral (P-I) filter, wherein the control logic of claim 32 is further limited to adapting the digital loop filter by updating a proportional coefficient and an integral coefficient of the digital loop filter. As claim 32 requires that these updates be driven by the average of the control values output by the claimed filter, the arguments given for the allowability of claim 12 over the combination of Tanaka and Glass apply with equal force to claim 33.

VIII. CLAIMS APPENDIX

The following claims are on appeal.

1. A method of generating an output clock signal from a phase-locked loop (PLL), the method comprising:

determining successive phase difference values between a reference clock signal and said output clock signal;

filtering said successive phase difference values to generate successive control values;

controlling a frequency of said output clock signal based on said successive control values; and

adapting a filter used to filter said successive phase difference values based on average control values determined from said successive control values.

2. The method of claim 1 further comprising detecting a trend in said average control values and determining a filter state based on said trend in said average control values.

3. The method of claim 2 further comprising selecting a fast filter setting for said filter when said trend indicates that said average control values have not stabilized.

4. The method of claim 2 further comprising selecting a slow filter setting for said filter when said trend indicates that said average control values have stabilized.

5. The method of claim 1 further comprising determining difference values between successive ones of said average control values, and wherein adapting said filter based on said average control values determined from said successive control values comprises adapting said filter based on processing said difference values.

6. The method of claim 5 wherein adapting said filter based on processing said difference values comprises:

integrating a number of said difference values to determine an integrated value of said number of said difference values; and

adapting said filter based on said integrated value.

7. The method of claim 6 wherein adapting said filter based on said integrated value comprises setting said filter to a slow filter state if said integrated value is below a defined threshold.

10. A method of controlling a phase-locked loop (PLL) to reduce clock deviations in an output signal generated by the PLL relative to clock deviations in an input reference timing signal to the PLL, the method comprising:

generating a phase error signal by determining a phase difference between said input reference timing signal and said output signal;

filtering said phase error signal with a digital filter to produce a digital control value;

determining average control values by averaging successive ones of said digital control value; and

adapting a filter characteristic of said digital filter based on said average control values.

11. The method of claim 10 wherein adapting said filter characteristic of said digital filter based on said average control values comprises:

adapting said digital filter such that relatively heavy filtering is applied to said phase error signal when successive average control values indicate a locked condition of the PLL; and

adapting said digital filter such that relatively light filtering is applied to said phase error signal when successive average control values indicate an unlocked condition of the PLL.

12. The method of claim 10 wherein said digital filter is a proportional-integral (P-I) digital filter and adapting said filter characteristic of said digital filter based on the average control values comprises changing a value of a proportional digital filter coefficient K_p and an integral digital filter coefficient K_i.

13. The method of claim 10 wherein adapting said filter characteristic of said digital filter based on said average control values comprises:

determining difference values between successive ones of said average control values;

integrating said difference values to determine an integrated value; and

adapting said filter characteristic of said digital filter based on said integrated value.

14. The method of claim 13 wherein said adapting said filter characteristic of said digital filter based on said integrated value comprises changing from a relatively slow filter time constant to a relatively fast filter time constant if said integrated value is above a first integrated value threshold.

15. The method of claim 14 further comprising changing back to said relatively slow filter time constant if said integrated value falls below a second integrated value threshold.

16. The method of claim 15 further comprising changing back to said relatively slow filter time constant if said integrated value does not fall below said second integrated value threshold after a defined duration of time.

18. The method of claim 13 further comprising entering a locked state of operation for said PLL if said integrated value is below a locked state integrated value threshold.

24. A phase-locked loop comprising:

a controllable oscillator providing an output signal from the PLL at a frequency proportionate to an oscillator control signal;

a phase detector providing a phase error signal by detecting a phase difference between an input signal and said output signal;

an adjustable loop filter providing control values based on filtering said phase error signal;

a control circuit providing the oscillator control signal responsive to said control values; and

control logic to control a filter characteristic of said loop filter based on an average control value determined from successive ones of said control values to minimize clock deviations in said output signal.

25. The phase-locked loop of claim 24 wherein said control logic is operable in one of a defined number of states, and further wherein said control logic adjusts said filter characteristic of said loop filter based on a current state of said control logic.

26. The phase-locked loop of claim 25 wherein said control logic transitions from a first state to a second state based on at least one characteristic of said average control values.

32. The phase-locked loop of claim 24 wherein said loop filter comprises a digital loop filter adapted to output said control value in a digital format.

33. The phase-locked loop of claim 32 wherein said digital loop filter is a proportional-integral (P-I) filter, and further wherein said control logic is adapted to update a proportional coefficient and an integral coefficient to effect changes in said at least one filter characteristic.

34. The phase-locked loop of claim 24 wherein said control circuit is a digital-to-analog converter (DAC), and further wherein said control value provided by said loop filter is a digital value conforming to an input range of said DAC such that said DAC generates a control voltage as said oscillator control signal relative to said digital value.

35. The phase-locked loop of claim 34 wherein said controllable oscillator is a voltage-controlled oscillator (VCO), and further wherein said VCO generates said output signal at a frequency determined by a value of said control voltage generated by said DAC.

37. The phase-locked loop of claim 24 wherein said control operates in one of a defined number of states, with each of said states corresponding to a desired filter setting for said loop filter, and to control transitions between said states based on processing average control values determined from said control values.

39. The phase-locked loop of claim 24 wherein said control logic comprises a digital processor.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.

Respectfully submitted,

COATS & BENNETT, P.L.L.C.

By: 

Michael D. Murphy
Registration No. 44,958
P.O. Box 5
Raleigh, NC 27602
Telephone: (919) 854-1844